A 1-V 3.8–5.7-GHz Wide-Band VCO With Differentially Tuned Accumulation MOS Varactors for Common-Mode Noise Rejection in CMOS SOI Technology

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***Abstract*—In this paper, a 1-V 3.8–5.7-GHz wide-band voltage-controlled oscillator (VCO) in a 0.13-μm silicon-on-insulator (SOI) CMOS process is presented. This VCO features differentially tuned accumulation MOS varactors that: 1) provide 40% frequency tuning when biased between 0–1 V and 2) diminish the adverse effect of high varactor sensitivity through rejection of common-mode noise. This paper shows that, for differential *LC* VCOs, all low-frequency noise such as flicker noise can be considered to be common-mode noise, and differentially tuned varactors can be used to suppress common-mode noise from being upconverted to the carrier frequency. The noise rejection mechanism is explained, and the technological advantages of SOI over bulk CMOS in this regard is discussed. At 1-MHz offset, the measured phase noise is −121.67 dBc/Hz at 3.8 GHz, and −111.67 dBc/Hz at 5.7 GHz. The power dissipation is between 2.3–2.7-mW, depending on the center frequency, and the buffered output power is −9 dBm. Due to the noise rejection, the VCO is able to operate at very low voltage and low power. At a supply voltage of 0.75 V, the VCO only dissipates 0.8 mW at 5.5 GHz.**

***Index Terms*—CMOS, common-mode noise rejection, differential tuning, flicker noise, MOS varactor, phase noise, RF, silicon-on-insulator (SOI), voltage-controlled oscillator (VCO), wide-band.**

I. Introduction

As MODERN CMOS technology feature size is scaled down to deep submicrometer, very thin gate oxide is required to maintain short-channel effects at an acceptable level. This leads to low breakdown voltage of the device and, therefore, the supply voltage V_{DD} has to decrease in proportion. The lowering of V_{DD} reduces power dissipation of digital circuits, but imposes many challenges to analog/RF designs [3], and the voltage-controlled oscillator (VCO) is no exception. The most obvious problem is the reduction of voltage swing, which lowers the output power and degrades the phase noise, as described in Leeson's formula [4]. This can be partially resolved by using a complementary topology to improve the phase noise [5].

Another problem, which is often overlooked, is the frequency-tuning range. A limited frequency-tuning range has always been a notorious problem for VCOs in CMOS technology. Varactors using reverse-biased diode junction capacitance from a p^+/n-well gives limited tuning range around a few percent and poor Q around 20 at 1 GHz [6]. The lowering of the voltage supply due to technology scaling further complicates the tuning problem. For example, as the technology advances from 0.35- to 0.13-μm lithography, the maximum supply V_{DD} drops from 3.3 to 1.2 V. The range of the varactor control voltage decreases accordingly, resulting in reduced frequency tuning range if the varactor gain remains the same. Therefore, for low-voltage CMOS VCOs to achieve respectable performance, a high-Q and high-sensitivity varactor is required.

The accumulation MOS (AMOS) varactor [7]–[9] offers a solution to this problem. High-Q AMOS varactors giving $C_{\max}/C_{\min}$ of five with ±1-V tuning voltage have been demonstrated in a 0.13-μm silicon-on-insulator (SOI) CMOS technology [1], and a VCO with over 50% frequency tuning[1] was measured [10] using this technology. However, a high $C_{\max}/C_{\min}$ ratio over a low voltage tuning range implies high varactor sensitivity k_v, which is unfavorable to phase noise performance, as described by the modified Leeson's formula [12], [13]

$$L(\Delta f, k_v) = 10\log\left\{\left(\frac{f_o}{2Q\Delta f}\right)^2\left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{\Delta f}\right)\right] + \left(\frac{k_v v_n}{2k_{LC}\Delta f}\right)^2\right\} \quad (1)$$

[1]The typical tuning range of a VCO is 15%–20% to cover process and temperature variation. A wide-band VCO like this can be used for dual-band operation, such as local oscillator (LO) frequency generation of both 2.4- and 5-GHz band for IEEE 802.11a and IEEE 802.11b wireless local area network (WLAN) application.

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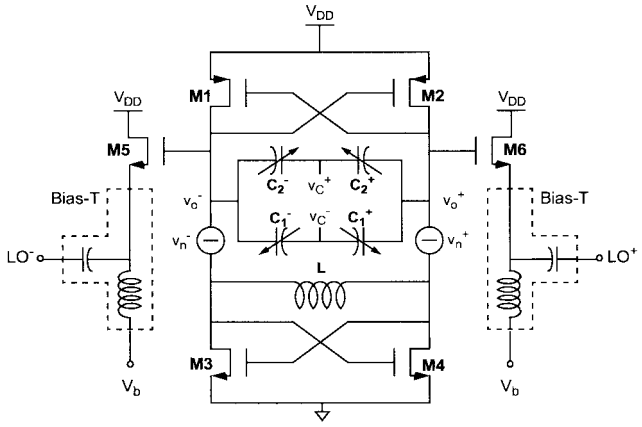

Fig. 1. Schematic of differentially tuned VCO. v_n^+ and v_n^- are noise sources from each branch.

where f_o is the frequency of oscillation, Q is the quality factor, Δf is the frequency offset from the carrier, F is the noise factor of the amplifier gain element, k is the Boltzmann's constant, T is the temperature, P_o is the RF power produced by the VCO, f_c is the flicker noise corner frequency, and k_{LC} is a constant that is a function of L and C in the resonator. A band-switching topology can be employed to reduce the effect of k_v while maintaining the required frequency tunability [10], but extra control circuitry is required to control the switching varactors, which complicates the phase-locked loop (PLL) locking procedure.

Differential tuning [11], as described in this paper, provides a simple, but effective solution to avoid the drawbacks of high k_v effect. In Section II, a simple theory will be introduced to explain how varactors upconvert low-frequency common-mode noise, such as flicker noise, near the carrier frequency, and how differentially tuned varactors can be used to suppress such upconversion. Section III describes the circuit and technology used for VCO implementation, including the measured data of the inductor and AMOS varactor used in the *LC* resonator. Furthermore, common-mode noise rejection performance of both SOI and bulk AMOS varactors are compared. Section IV contains experimental results for theory verification. Finally, this paper is summarized and concluded in Section V.

II. Noise Analysis

A. Low-Frequency Noise Upconversion

One mechanism for upconversion of low-frequency noise, such as flicker noise, is the nonlinearity of the circuit [5]. However, the low-frequency noise can also modulate the varactor directly and this is seen as jitter near the carrier. Consider a complementary *LC* VCO, as shown in Fig. 1. The resonator consists of the inductor L and the capacitor C, which consists of C_1^+, C_1^-, C_2^+, and C_2^-. The resonant frequency ω_o is given by

$$\omega_o = \frac{1}{\sqrt{LC}}. \tag{2}$$

Consider v_n^+ and v_n^- (shown in Fig. 1) as the total noise at the resonator terminals from the transistors at each branch. Note that, at low frequency, the inductor L behaves like a short circuit.[2] Therefore, all the noise power at low frequency can be considered as common-mode noise, defined as $v_{\rm ncm}$, such that

$$v_{\rm ncm} = \sqrt{\overline{\left(v_n^+ + v_n^-\right)^2}}. \tag{3}$$

One mechanism for low-frequency noise upconversion is that $v_{\rm ncm}$ injects into the varactor through the nodes v_o^+ and v_o^-. This noise is subsequently upconverted to the carrier frequency by modulating the resonator, contributing to the phase noise of the VCO. Mathematically, C in (2) can be expressed as

$$C = C_0 + k_v(v_C + v_{\rm ncm}) \tag{4}$$

where C_0 is the zero bias capacitance, k_v is the varactor sensitivity, and v_C is the control voltage of the varactor. Equation (4) clearly shows that C is modulated by $v_{\rm ncm}$, and the higher the k_v, the worse the low-frequency noise injection. Therefore, many VCOs have the worst phase noise in the middle of the tuning range where k_v is the highest. Meanwhile, the best phase noise is usually achieved at the boundaries of the tuning range where k_v is minimum. As the voltage supply scales down, high varactor sensitivity k_v is required to maintain the same tuning range. Therefore, this upconversion mechanism is critical for a low-voltage VCO.

B. Noise Rejection With Differentially Tuned Varactor

The concept behind common-mode noise rejection in a differentially tuned varactor is analogous to power-supply rejection in differential circuits [14]. The differentially tuned varactor topology consists of two pairs of varactors. One pair is RF excited at the cathode (C_1^+ and C_1^-) and the other pair is excited at the anode (C_2^+ and C_2^-).[3] The schematic and the associated *C–V* characteristics are shown in Fig. 2. From the *C–V* curve, any common-mode noise introduced by one pair will be cancelled by its dual counter pair, preventing the noise from modulating the varactor. Mathematically, for a single-ended varactor, the equivalent capacitance C between v_C and v_o^+ is calculated from (4) and is given by

$$C = 2C^+ = 2C_0 + 2k_v(v_C + v_{\rm ncm}). \tag{5}$$

As expected, the common-mode noise modulates the varactor, which will result in jitter and phase noise. For differentially tuned varactors, the capacitances are given by v_C^+, v_C^-, and v_o^+ such that

$$C_1^+ = C_0 + k_{v1}(v_C^+ + v_{\rm ncm}) \tag{6}$$

$$C_2^+ = C_0 - k_{v2}(v_C^- + v_{\rm ncm}). \tag{7}$$

Since $C = C_1^+ + C_2^+$, if the varactor is perfectly symmetrical such that $k_{v1} = -k_{v2}$, the expression for C is

$$C = 2C_0 + 2k_v v_C \tag{8}$$

where v_C is $v_C^+ - v_C^-$, and all the common-mode noise $v_{\rm ncm}$ is rejected. If $|k_{v1}|$ and $|k_{v2}|$ are not the same, the gain of the common-mode noise is $|k_{v1} - k_{v2}|$.

[2]For this design, the impedance of the resonator is less than 0.004 Ω below 1 MHz.

[3]Varactor excitation will be explained in Section III.

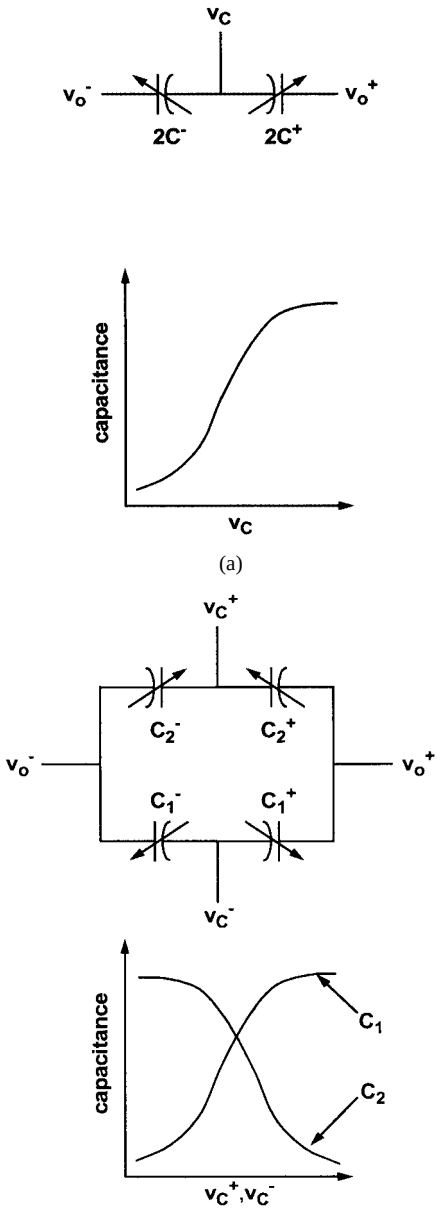

Fig. 2. (a) Single-tuned and (b) differentially tuned varactor.

In summary, it has been shown that differential tuning can be used to reject common-mode noise, reducing the upconversion of low-frequency noise, such as flicker noise and shot noise, which would have been upconverted near the carrier through varactor modulation.

III. Design and Technology

As shown in Fig. 1, the VCO is an *LC* cross-coupled differential circuit with both PMOS and NMOS latches, which generate negative resistance to cancel losses in the *LC* resonator. The AMOS varactors are differentially tuned for common-mode noise rejection, and the key for good noise rejection is varactor symmetry. A varactor is perfectly symmetrical if

$$C_{gg}(v_{C0}+v_C)=C_{ss}(v_{C0}-v_C) \tag{9}$$

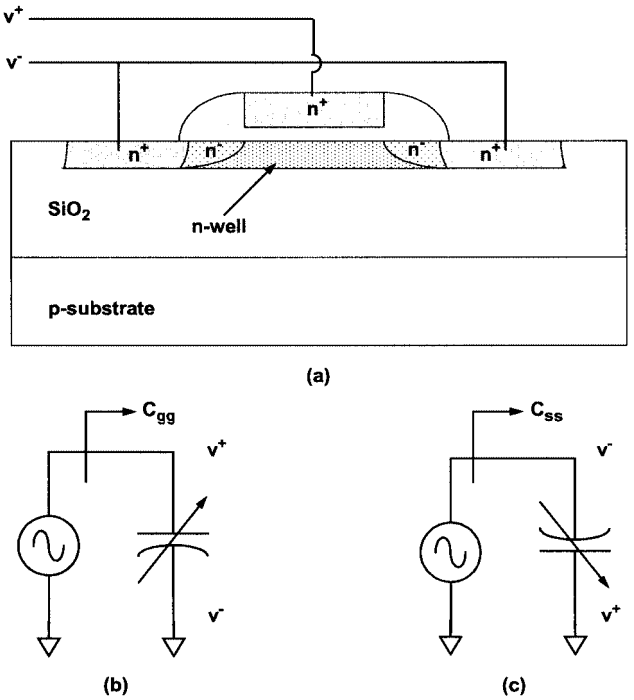

Fig. 3. (a) n-type AMOS varactor structure. (b) Cathode excitation. (c) Anode excitation.

where v_{C0} is a constant voltage that gives nominal capacitance C_0, and v_C is the control voltage. C_{gg} is the device capacitance when the varactor is operated with the diffusion (source and drain) and substrate[4] terminals shorted together and an RF small-signal applied to the gate [cathode excitation, Fig. 3(b)]. If the small-signal RF input is applied to the diffusion with all other terminals grounded, the capacitance is C_{ss} [anode excitation, Fig. 3(c)]. C_{ss} is always larger than C_{gg} since the former includes extrinsic capacitance between the diffusion and substrate C_{sb}.

SOI offers much better device symmetry compared to bulk technology. Consider the cross sections of an n-type AMOS varactor in both technologies, as shown in Fig. 4. While C_{sb} of SOI is the buried oxide capacitance $C_{\rm box}$ underneath the active area, the substrate capacitance for bulk is the depletion capacitance of the n-well. Instead of a fixed high-Q capacitor as in SOI, the depletion capacitance is a reverse pn junction that behaves as a low-Q voltage-dependent varactor. Hence, this parasitic diode not only lowers the Q, but also couples substrate noise to the resonator, degrading the phase noise of the VCO.

The measured *C–V* characteristic at 1 GHz are shown in Fig. 5. The varactor has a $C_{\max}/C_{\min}$ about six over a tuning voltage of ± 1 V, and C_{gg} is virtually the mirror image of C_{ss}, as described in (9). Therefore, varactors in SOI are highly symmetrical, and are more suitable for implementation as differentially tuned varactors than AMOS varactors offered in bulk technology.

The monolithic inductor is a horseshoe-shaped single loop with a diameter of 460 μm, as shown in the micrograph. The measured inductance is 0.85 nH and Q is above 20 between

[4]Substrate node for bulk technology only.

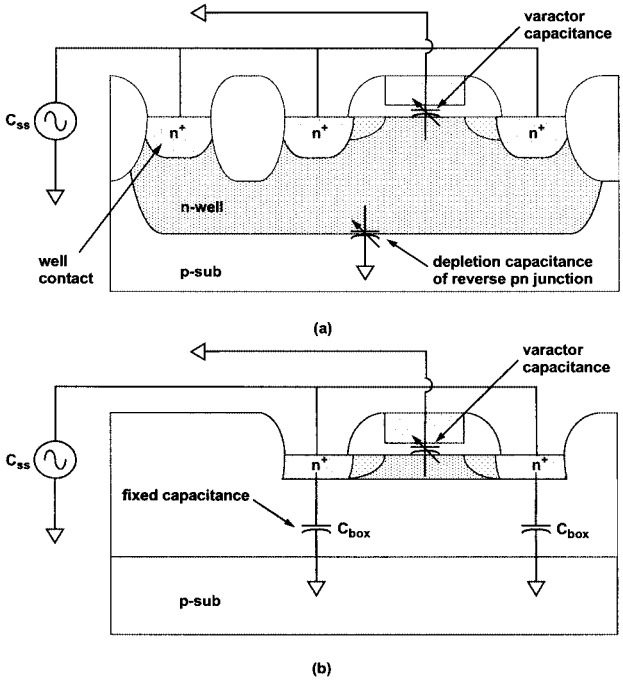

Fig. 4. Cross section and extrinsic capacitances of AMOS varactor in: (a) bulk and (b) SOI technology.

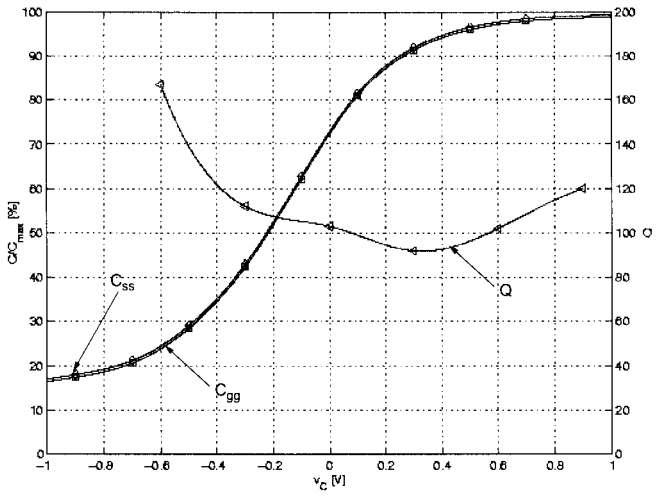

Fig. 5. Measured varactor *C–V* and *Q–V* (of C_{gg}) characteristics at 1 GHz.

3.8–5.7 GHz, as shown in Fig. 6. The inductor is fabricated in a standard digital copper process.

The VCO uses bias-T source followers as the output buffers. The inductive choke inside the bias-T is used to provide high ac impedance and stability for the source follower. Hence, small transistors can be used to provide enough output current drive without loading the VCO core heavily. Finally, for demonstration purpose only, transistor sizing was used to control the VCO current instead of using a current source.

IV. Experimental Results

A. Frequency Tuning

The VCO was measured using wafer probing together with a 26.5-GHz HP8563 spectrum analyzer with a phase-noise module. The dependence of frequency on varactor tuning

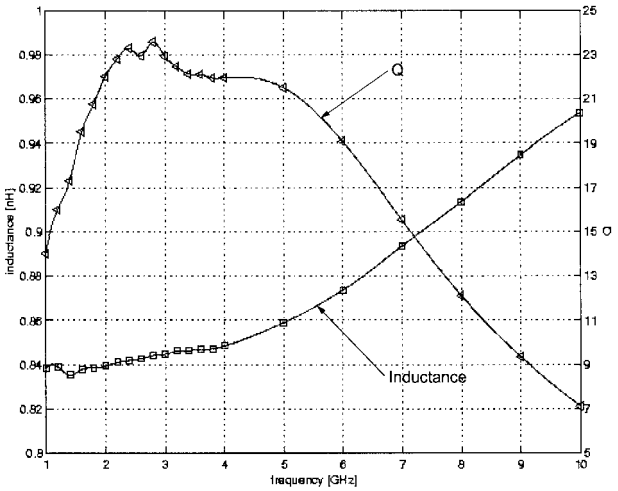

Fig. 6. Measured single-ended measurement of horseshoe inductor.

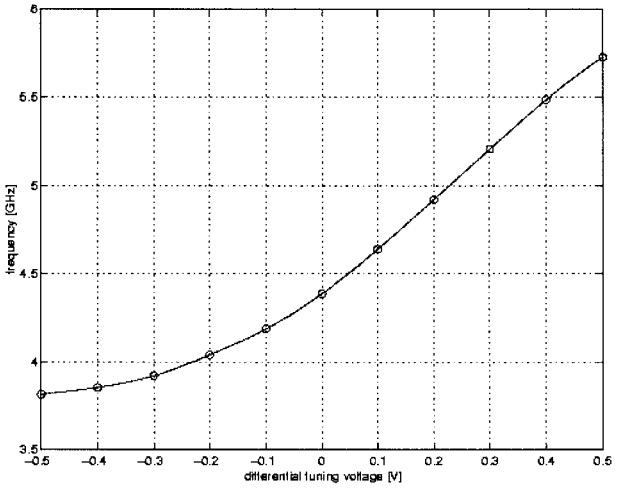

Fig. 7. Frequency versus tuning voltage at 1-V V_{DD} of differentially tuned VCO.

voltage at 1-V V_{DD} is shown in Fig. 7. The differential tuning voltage $v_{\rm dtune}$ is related to v_C^+ and v_C^- by

$$v_C\pm = \left(\frac{V_{DD}}{2}\right) \pm v_{\rm dtune}. \tag{10}$$

For example, if $v_{\rm dtune}$ is 0 V, then v_C^+ is 0.5 V and v_C^- is 0.5 V. If $v_{\rm dtune}$ is -0.5 V, then v_C^+ is 0 V and v_C^- is 1 V. For a tuning voltage between 0–1 V, the carrier frequency can be tuned from 3.812 to 5.716 GHz, achieving a 40% tuning range. This wide tuning range is made possible by the high $C_{\max}/C_{\min}$ ratio of the AMOS varactor. Note that while many low-voltage VCOs [10][15][16] use higher voltages to achieve the required frequency tuning, this differentially tuned VCO only requires $\pm$0.5 V, making it a true 1-V oscillator.

B. Common-Mode Rejection Ratio (CMRR)

The common-mode rejection of the varactor was measured. At 1-V V_{DD}, a common-mode voltage was applied such that $v_C^+ = v_C^-$, and the result is summarized in Table I. The frequency variation is within 2%, while the phase-noise variation is within $\pm$1 dB. Therefore, it is concluded that the varactors are highly

TABLE I
COMMON-MODE PERFORMANCE MEASUREMENT

$v_C^+ = v_C^-$	f_c	phase noise @ 1-MHz offset
0.0 V	4.492 GHz	−117.00 dBc/Hz
0.5 V	4.401 GHz	−117.83 dBc/Hz
0.6 V	4.404 GHz	−118.33 dBc/Hz
1.0 V	4.475 GHz	−118.50 dBc/Hz

symmetrical, which should result in good common-mode noise rejection. A figure-of-merit (FOM) is introduced to provide a numerical standard for the performance of common-mode rejection. In analog circuit design, CMRR [14] is defined as

$$\text{CMRR} = \frac{A_d}{A_c} \tag{11}$$

where A_d is the differential gain, and A_c is the common-mode gain. A_d is similar to k_v, which can be extracted from the frequency-voltage curve shown in Fig. 7. Meanwhile, A_c is estimated from the frequency deviation from the common-mode measurement, defined as

$$k_{vCM} = \frac{\text{maximum change in } f_c}{\text{change in } v_C}. \tag{12}$$

In this design, maximum change in center frequency is 4.492–4.401 GHz, which is 0.091 GHz, and the change in v_C is 0.5 V, therefore the common-mode varactor sensitivity is 0.182 GHz/V. Hence, the CMRR is

$$\text{CMRR} = 20 \cdot \log\left(\frac{k_v}{k_{vCM}}\right) \tag{13}$$

which gives 20 dB. Thus, the upconverted noise is expected to be suppressed by 20 dB.

C. Phase Noise

The phase noise was measured at several different frequencies across the wide tuning range. At 1-V V_{DD}, the best phase noise is −121.67 dBc/Hz at 1-MHz offset, measured at the lower frequency bound (3.812 GHz at v_{dtune} of −0.5 V), where the VCO sensitivity is minimal and the inductor Q is near its peak. At the middle of the range (4.4 GHz at v_{dtune} of 0 V), k_v is high and the phase noise is −117.83 dBc/Hz at 1-MHz offset. At the upper end of the tuning range (5.716 GHz at v_{dtune} of 0.5 V), the phase noise is −111.67 dBc/Hz at 1-MHz offset. The phase noise was also measured for V_{DD} between 0.75–1.4 V, and the results are summarized in Fig. 8.

To evaluate the phase-noise improvement of differential tuning over a conventional single-ended tuning scheme, a reference VCO with the same inductor and transistors, but a single-ended varactor topology, as shown in Fig. 2(a), was fabricated and measured. At 4.4 GHz, with both VCOs operating in the high k_v region (middle of the tuning range), the phase noise was measured and compared, as shown in Fig. 9. At 1-MHz offset, the differential-tuning topology improves the phase noise by approximately 9 dB. Due to common-mode rejection, the upconverted low-frequency noise near the 100-kHz offset is filtered out, offering a cleaner frequency spectrum.

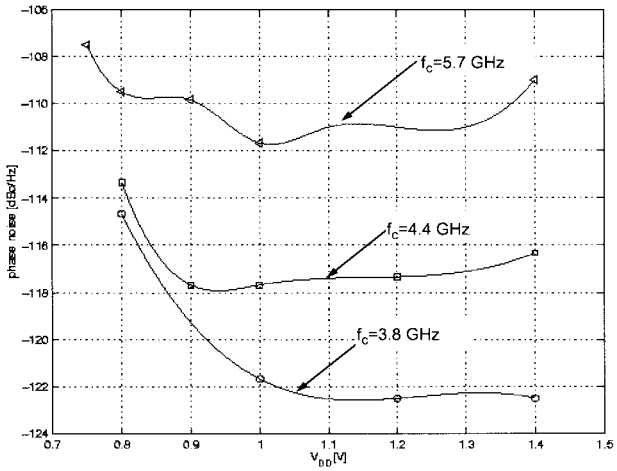

Fig. 8. Phase noise versus V_{DD} differentially tuned VCO.

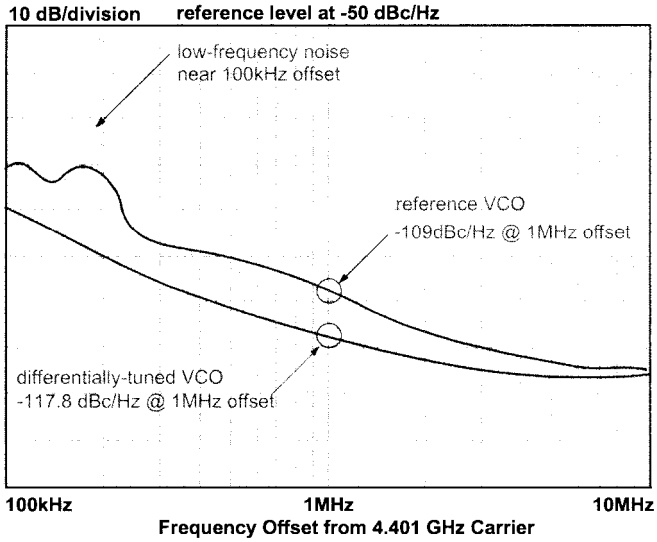

Fig. 9. Phase-noise comparison at 4.4 GHz.

The comparison is summarized in Table II. At low k_v, where the *C–V* curve is nearly flat, the lowest phase noise is measured for both VCOs. As the operation moves to the mid-rail, the varactor sensitivity increases, and the phase noise degrades due to noise injection and higher frequency of oscillation, as predicted by (1). However, despite a higher k_v, the phase-noise degradation is not as severe as in the reference VCO. This clearly demonstrates the effectiveness of noise rejection of the differentially tuned VCO.

D. Power Dissipation and VCO FOM

The dc power dissipation P_{dc} is plotted in Fig. 10, and the VCO FOM is defined as

$$\text{FOM} = L\{\Delta f\} - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{\text{dc}}}{1\text{ mW}}\right) \tag{14}$$

where $L\{\Delta f\}$ is the measured phase noise at the frequency offset Δf from the carrier at f_o, and P_{dc} is the measured dc power dissipation in milliwatts, as plotted in Fig. 11. The reference VCO dissipated 2–3 mW depending on the frequency of

TABLE II
PERFORMANCE SUMMARY OF SINGLE-ENDED AND DIFFERENTIAL VARACTORS

design	frequency f_o [GHz]	sensitivity k_v [GHz/V]	phase noise [dBc/Hz]
reference [10]	3.0	0.0	−120.8
	4.4	2.0	−109.0
differentially-tuned	3.8	0.0	−121.7
	4.4	2.4	−117.8

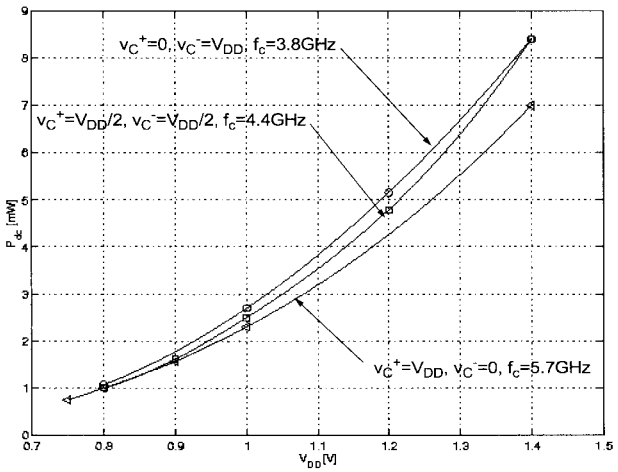

Fig. 10. DC power dissipation of differentially tuned VCO.

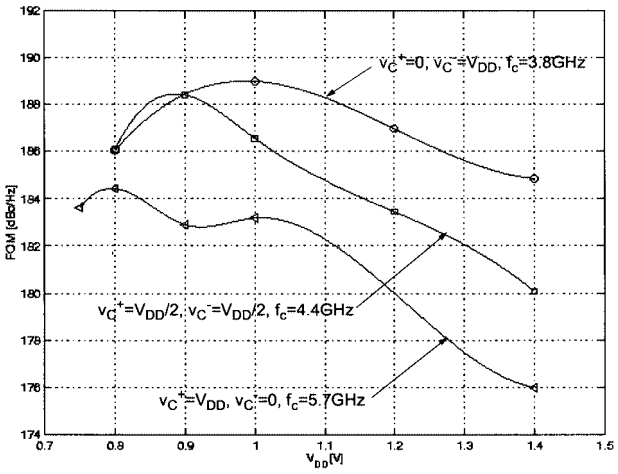

Fig. 11. FOM measurement of differentially tuned VCO.

operation, which is approximately the same as the differentially tuned topology. The output power for both VCOs are −9 dBm. The differentially tuned VCO has the lowest power dissipation achieved at 0.75-V V_{DD}, where only 0.8 mW of power is drawn at 5.5 GHz, with the output power of −14 dBm. To the author's knowledge, this VCO has the lowest power dissipation compared to any published CMOS VCO at this frequency. Meanwhile, the reference VCO can only operate down to 0.83 V, drawing approximately 1 mW at that frequency. The best FOM is −189 dBc/Hz achieved at 1-V V_{DD}.

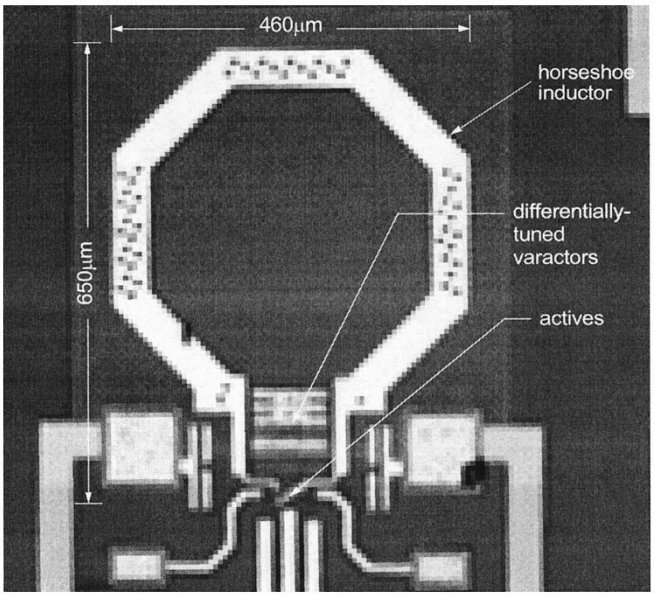

Fig. 12. Micrograph of differentially tuned VCO.

V. SUMMARY

In this paper, the design and measured characteristic of differentially tuned complementary *LC* VCOs with 40% tuning range has been presented. The VCO has demonstrated that differentially tuned varactors can provide wide tuning range and reject common-mode noise. The buried oxide of SOI makes AMOS varactors higher Q and more symmetric than those in bulk technology, and this has the significant advantage for common-mode rejection in a differentially tuned topology. At 1-V V_{DD} and 1-MHz offset, the nominal phase noise (4.4 GHz at v_{dtune} of 0 V) is −117.83 dBc/Hz and the FOM is 187 dBc/Hz. The power consumption is between 2.3–2.7 mW, and the buffered output power is −9 dBm. If the VCO is operated at 0.75-V V_{DD}, the circuit only draws 0.8 mW of power, the lowest power dissipation of any published CMOS VCO. The VCO occupies a total area of 650 μm × 460 μm, excluding the pads, as shown in the micrograph of Fig. 12.

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